

# **Pi 2 Media**

**503HTA  
Hybrid Tube Amp Hat  
Hardware Reference Manual  
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## I WARRANTY

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This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life-sustaining or life-saving product and this warranty is not applicable nor is Pi 2 Design liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Pi 2 Design expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

## 2 OPERATING SPECIFICATIONS

### 2.1 503HTA OPERATING SPECIFICATIONS

The 503HTA conforms to the following specifications:

Specification	Value
Dimensions	65mm x 56.5mm – Hat Compliant
Weight	~8oz (with tube)
Storage Temperature	0C to +70C
Operating Temperature	0C to +50C
Humidity	0% to 95% RH, Non-Condensing
Input Voltage (VIN)	+24V +/- 5% 1A Peak
Power Consumption	8W Typical, 10W Maximum

Table 1 – 503HTA Operating Specifications

## 3 OVERVIEW

### 3.1 INTRODUCTION

The 503HTA, designed and manufactured by Pi2Media (a division of PI 2 Design), is a High Quality I/O Shield designed to bring “Sweet Tube Sound” to the Raspberry Pi® family of Single Board Computers. This HAT allows the Raspberry Pi® SBC to drive Headphones from 32 - 300 ohm with ease and fidelity.

The On-Board PCM5102A, 24-Bit @ 192Khz DAC drives the single stage Dual Triode Tube. The Class-A Output Buffer consists of the Audiophile grade IRL510 MOSFET and LM317A Constant Current Source. A dedicated 6.3V Heater supply insures lowest crosstalk.

In addition, the 503HTA can be operated as a Stand Alone Headphone Amp via the 3.5mm Line In jack. The major features of the 503HTA are as follows:

- **FORM FACTOR** – Raspberry Pi® HAT Compliant Size w/40-Pin mating connector
- **24-Bit DAC** – The well regarded -112db THD PCM5102 is used to convert the I2S Stream to drive the Single Triode Tube Stage at 24-Bit up to 192Khz Frame Rate
- **TUBE ROLLING** – The 503HTA supports both 6DJ8 (default is JJ 6DJ8) and 12AU7 type tubes. Individual Anode Bias Adjustment Pots plus selectable Series/Parallel Heater Configuration insure the perfect setup for virtually any tube!
- **HEADPHONE OUT** – Rugged 3.5mm Jack plus selectable output resistance between 1.5, 32 and 100 ohms.
- **VOLUME POT AND GAIN SELECT** – High Quality ALPS Potentiometer and Dual Gain settings allow the user to select the output voltage to the optimal level for each Headphone.
- **SINGLE POWER INPUT** – A Single 24V @ 2A input powers the 503HTA as well as the attached PI, providing 5V @ 3A.
- **STAND ALONE OPERATION** – The 503HTA can also be operated in stand-alone mode using the 3.5mm Line In Jack.

### 3.2 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the 503HTA HAT.

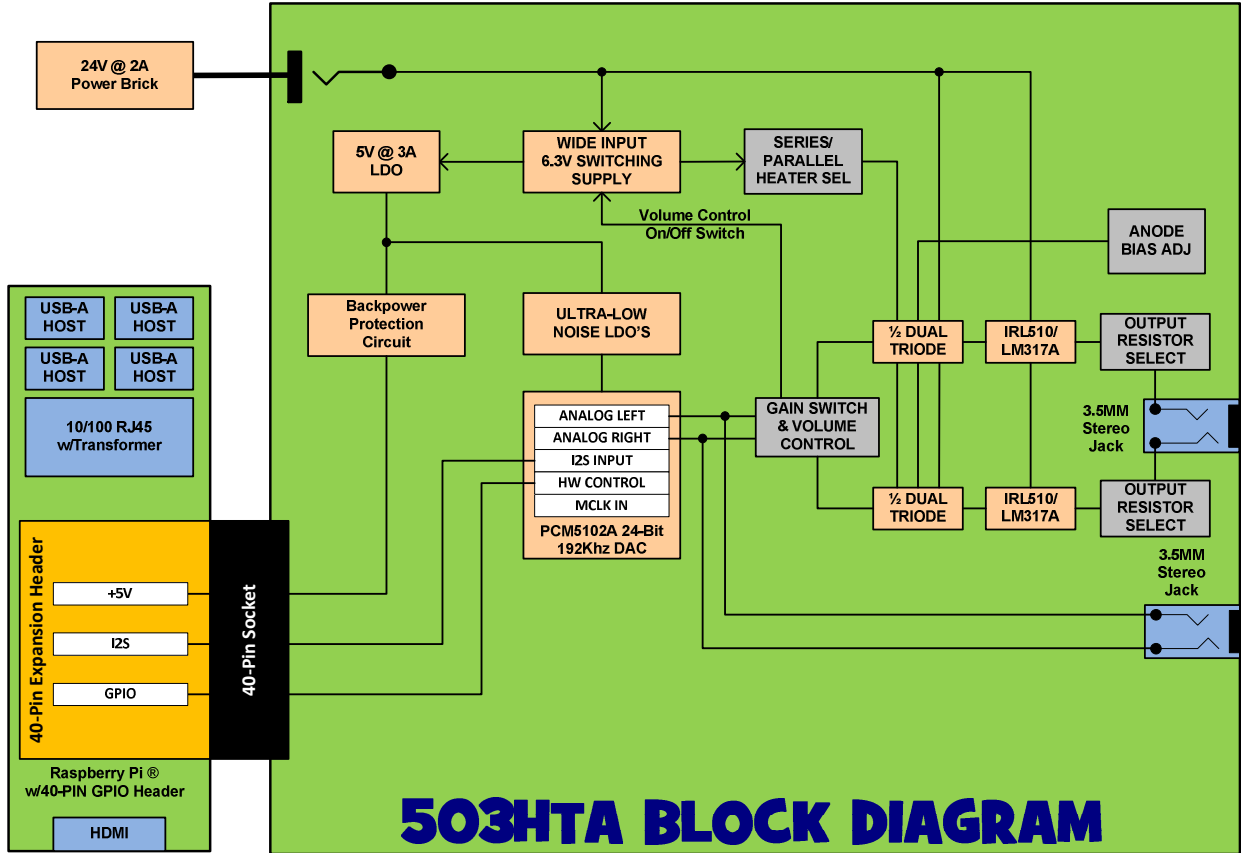


Figure 1 – 503HTA Block Diagram

# 4 ON-BOARD FUNCTIONS

## 4.1 OVERVIEW

The 503HTA interfaces to the RPi via the 40-Pin GPIO Connector. This section describes in detail the functionality located on the 503HTA.

### 4.1 PCM5102A 24-BIT 192KHZ DAC

At the core of the 503HTA is the Texas Instruments PCM5102A 24-Bit 192Khz DAC. This device interfaces to the Raspberry Pi via the I2S. The signals used to interface with the PCM5102A are shown in the following table.

PCM5102A Signal	RPi Signal	Description
MCLK	-	Grounded at PCM5102A
BCLK	BCLK	I2S Bit Clock from Pi
LRCLK	LRCLK	I2S Word Clock from Pi
SDIN	SDOUT	I2S Serial Audio Data from Pi
DEMP	GPIO13	Pulled High to Enable De-Emphasis, Drive Low to Disable
FILT	GPIO6	Pulled High to Enable Digital Filter, Drive Low to Disable
*MUTE	GPIO5	Pulled Low to Mute, Drive High to Enable

Table 2 – RPi to PCM5102A Connections

#### 4.1.1 PCM5102A 24-BIT 192KHZ DAC NOTES

1. The 503HTA is designed to operate the PCM5102A in PLL mode. In this mode the PCM5102A receives its master clock from an internal PLL using BCLK as the basis. The PCM5102A automatically detects the incoming frequency of BCLK and adjust its PLL accordingly.
2. The PCM5102A is Hardware controlled and thus has no direct SW visible functionality. But, three GPIO's (5, 6, and 13) are connected in order to control various options as described further below.
3. Although GPIO5 (MUTE) has a default pullup on the RPi of about 75K, which over-rides the 1Meg pulldown on the 503HTA, SW should drive this

pin high.

4. See the PCM5102A datasheet for more information on the FILT function controlled by GPIO6.
5. Software should drive GPIO13 low to disable De-Emphasis.
6. The DAC, when at maximum level, outputs 2Vrms to the Dual Triode Tube Amp.

## ***4.2 DUAL TRIODE AMPLIFIER***

A Dual Triode Amplifier provides the voltage amplification of the input signal (DAC or Line In). This circuit designed to provide 10db (3.3x) of overall gain (with volume control at 100%).

### ***4.2.1 DUAL TRIODE AMPLIFIER NOTES***

1. There is an attenuation switch which, when enabled (up position) reduces the input to the Amp by 10db, thus reducing overall maximum gain to 0db.
2. The Amp is driven from either the PCM5120A DAC or, when a plug is inserted, the 3.5mm Line In jack.
3. An ALPS 10K Dual Potentiometer provides volume control and a power on/off switch.
4. If the output is to be driven to a line level input on another device, the user should enable the high attenuation. With this enabled (switch up) and the volume control at 100% the overall gain is ~0db.

## ***4.3 CLASS-A MOSFET BUFFER***

A Class-A Buffer consisting of the IRL510 MOSFET and LM317 Constant Current Source provides up to 125ma (peak) of output current to drive Headphones from 32 to 600 ohm.

### ***4.3.1 CLASS-A MOSFET BUFFER NOTES***

1. A three position slide switch adds 0, 47 or 100 ohm in series with the output. This allows low ohm headphones to be driven with much lower noise and overall power consumption. For the best experience, the user should start at the highest resistance and reduce only if the output levels are not satisfactory.
2. There is a 25 second delay from power up before the headphone output is enabled. This allows the tube to warm up and reduces power on thumps. The output is disabled immediately when power is removed.

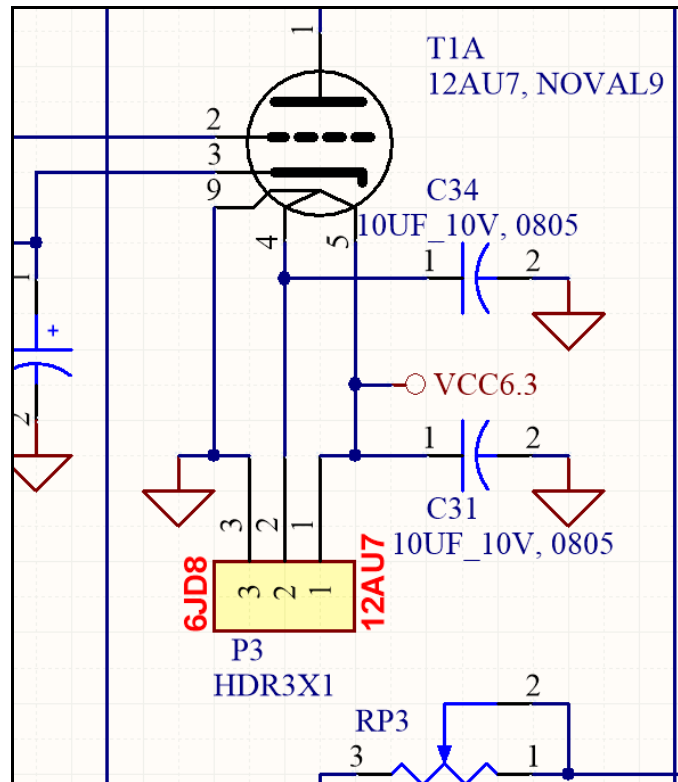


#### 4.4 6.3V HEATER SUPPLY

A low noise, high performance switching supply provides the 6.3V for the Tube Heaters. This supply also feeds the 5V LDO used to power the RPi (up to 3A).

##### 4.4.1 6.3V HEATER SUPPLY NOTES

1. A 3-Pin Jumper is used to select how the power to the Tube Heater is fed. In 6V mode a jumper is placed on pins 2-3, while in 12V mode a jumper is placed on pins 1-2. Note that 12V mode only works with tubes that allow 6.3V parallel operation, such as the 12AU7. The following circuit illustrates this:



# 5 RPI GPIO

## 5.1 OVERVIEW

The 503HTA uses a number of signals from the RPi GPIO header for control and status purposes. This usage is defined in the following table.

RPi PIN	DIR	AF	PUP/PDN	503HTA Name	Description/Notes
1	-	-	-	-	RPi +3.3V - Unused
2	-	-	-	+5V	+5V Power to/from the RPi
3	I/O	Y	PUP	I2C_SDA	I2C Bus Data - unused
4	-	-	-	+5V	+5V Power to/from the RPi
5	OUT	Y	PUP	I2C_SCL	I2C Bus Clock - Unused
6	-	-	-	GND	
7	-	-	-	GPIO4	Unused
8	-	-	-	GPIO14	Unused
9	-	-	-	GND	Unused
10	-	-	-	GPIO15	Unused
11	-	-	-	GPIO17	Unused
12	IN	Y	-	BCLK	I2S Bit Clock to pCM5102A
13	-	-	-	GPIO27	Unused
14	-	-	-	GND	
15	Out	-	-	GPIO22	Power Hold – Drive high to keep power on
16	-	-	-	GPIO23	Unused
17	-	-	-	-	RPi +3.3V - Unused
18	IN	-	PUP	GPIO24	Power Switch – Read state of power on/off switch. Low = on.
19	-	-	-	GPIO10	Unused
20	-	-	-	GND	
21	-	-	-	GPIO9	Unused

RPi PIN	DIR	AF	PUP/PDN	503HTA Name	Description/Notes
22	-	-	-	GPIO25	Unused
23	-	-	-	GPIO11	Unused
24	-	-	-	GPIO8	Unused
25	-	-	-	GND	
26	-	-	-	GPIO1	Unused
27	-	-	-	ID_SDA	Unused
28	-	-	-	ID_SCL	Unused
29	OUT	-	PUP	*MUTE	GPIO5, 0 = Mute PCM5102A Output
30	-	-	-	GND	
31	OUT	-	PUP	FILT	GPIO6, 1 = Enable PCM5102A Filter
32	-	-	-	GPIO12	Unused
33	OUT	-	-	DEMP	GPIO13, 1 = Enable De-Emphasis (44.1k only)
34	-	-	-	GND	
35	OUT	Y	-	LRCLK	I2S Left/Right Clock to PCM5102A
36	-	-	-	GPIO16	Unused
37	-	-	-	GPIO26	Unused
38	-	-	-	GPIO20	Unused
39	-	-	-	GND	
40	OUT	Y	-	SDOUT	Pi I2S Serial Audio Data to PCM5102A

Table 3 – CPU GPIO Pin Assignments

**5.1.1 RPI GPIO NOTES**

1. DIR is from the point of view of the RPi.
2. Y in the Alternate Function (AF) column indicates that the use of this pin requires the pin to be assigned to the function as defined by the RPi specifications.
3. PUP/PDN indicates if the GPIO should have its associated Pullup (PUP) or Pulldown (PDN) resistor enabled.
4. An asterisk ‘\*’ at the beginning of the name indicates a low true signal.

## 6 503HTA POWER

### *6.1 OVERVIEW*

The 503HTA is designed to be powered from an external 24V +/- 5% source via 5.5mm x 2.1mm Jack.

### *6.2 SOFTWARE CONTROLLED POWER HOLD*

GPIO22 allows the RPi to hold the power on even after the user turns the power switch to the off position. After initialization, software can drive PWR\_HLD (GPIO22) high, thus holding the power on regardless of the state of the on/off switch. Driving this low removes this hold condition. Note that for proper operation this requires user software to disable the internal pullup for GPIO22.

### *6.3 SOFTWARE VISIBLE POWER STATE*

The 503HTA allows the RPi to keep the system powered for clean shutdown. As part of this, PWR\_SW (GPIO24) is used to sense the state of the ALPS Volume Control Switch. When high it indicates that the user has turned the volume control all the way to the left (counter clockwise) and thus opened the on/off switch. Note that for proper operation this circuit requires user software to enable the internal pullup for GPIO24.

The following schematic illustrates the Power Hold Circuit:

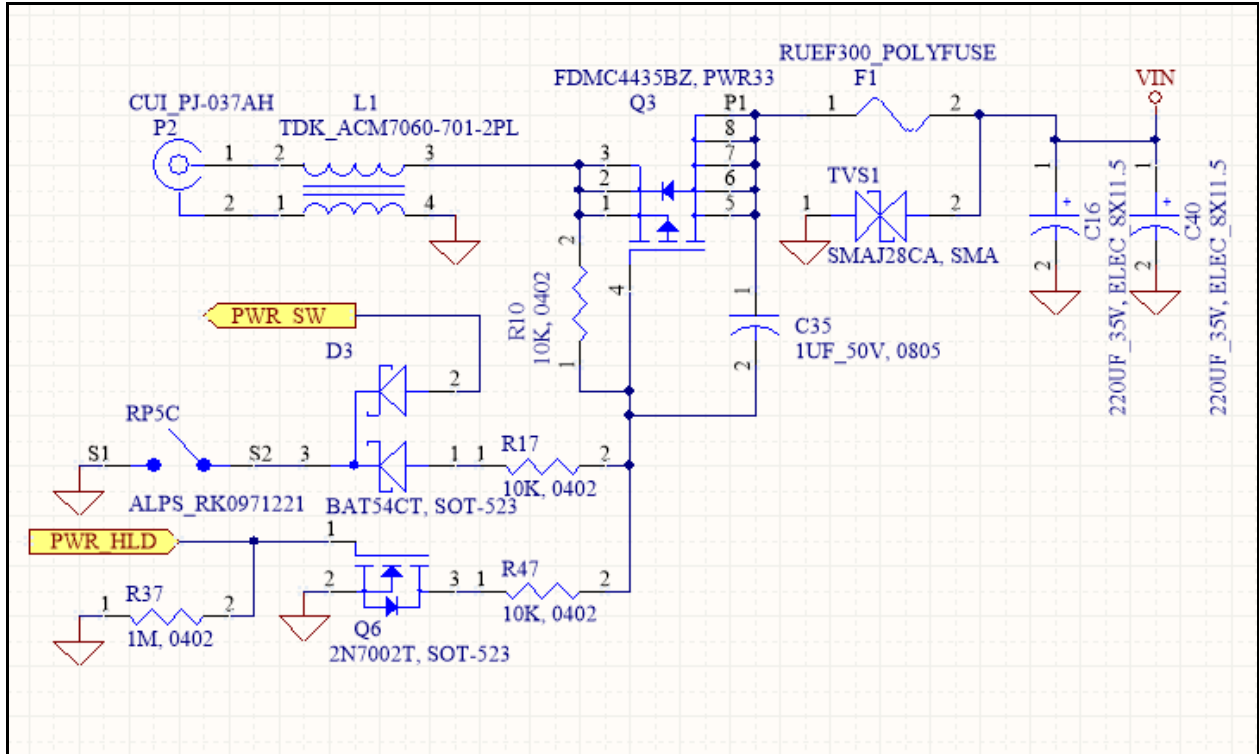


Figure 2 – 503HTA Power Hold Circuit

## 7 503HTA SOFTWARE

### *7.1 OVERVIEW*

Due to the various resources interfaced on the 503HTA, both internal and external to the RPi, it is necessary to initialize a large number of CPU registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. See our web site at <http://www.pi2design.com> or email us at [support@pi2design.com](mailto:support@pi2design.com) for example operating and initialization code.

# 8 CONNECTORS AND SWITCHES

## 8.1 OVERVIEW

This section provides the type, location and pinout for the various connectors and switches on the 503HTA Top Side. These are shown in the 3D rendering below.

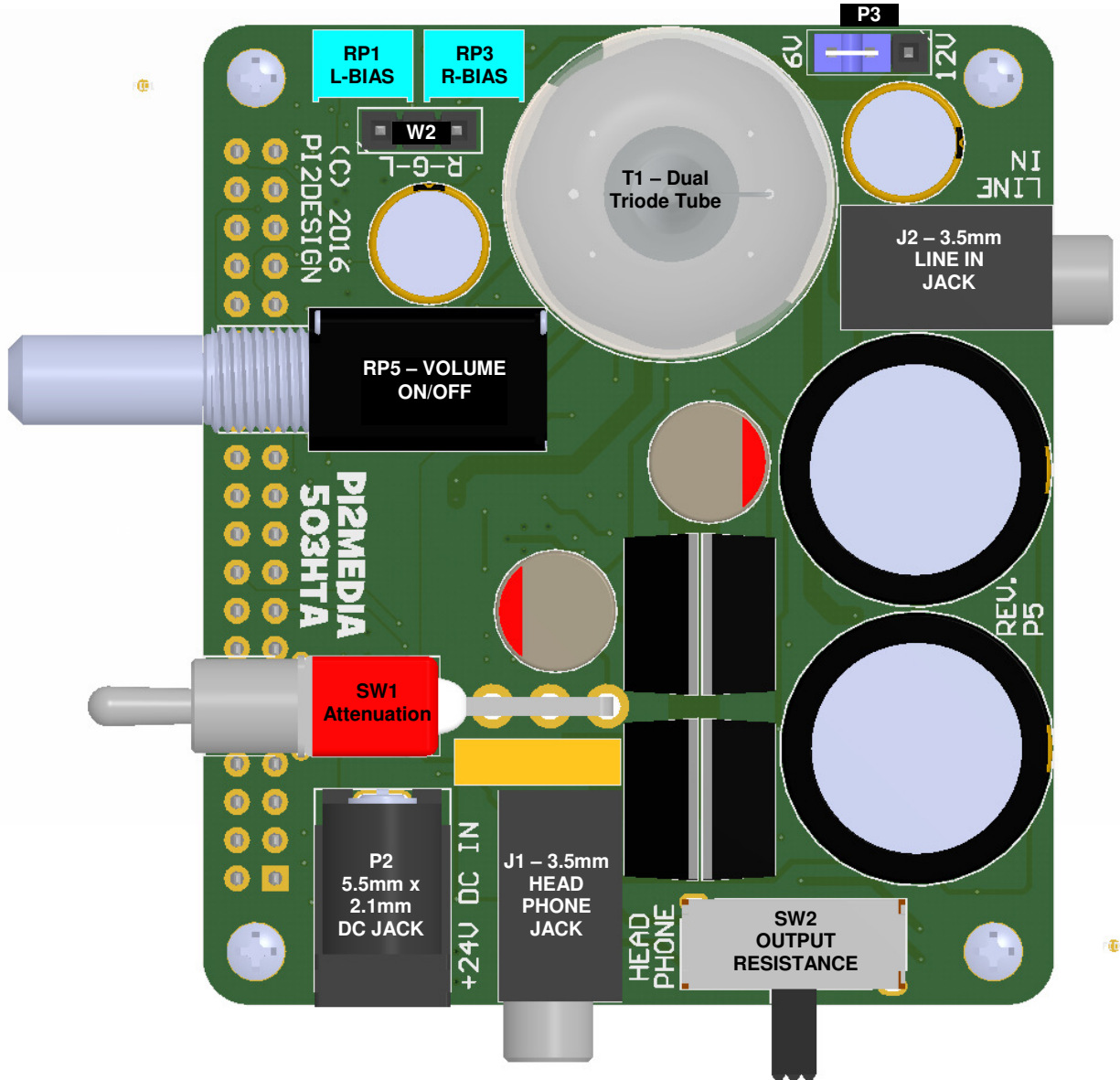


Figure 3 – 503HTA Connectors and Switches

## 8.2 P2 – DC JACK

This jack is designed to accept a 5.5mm x 2.1mm center positive plug for external power in. Voltage must be 24V +/- 5%, 2 Amp minimum.

### ***8.1 J1 – 3.5MM HEADPHONE JACK***

J1 is a 3.5mm Stereo Jack for Headphone Out

### ***8.2 J2 – 3.5MM HEADPHONE JACK***

J2 is a 3.5mm Stereo Jack for Line In

### ***8.3 W2 – 3-PIN BIAS ADJUST HEADER***

W2 is a 3-pin .1" single row header. It allows access to the Left and Right Channel Bias points. The pins are marked R-G-L for Right, Ground and Left respectively.

### ***8.4 P3 – 3-PIN HEATER VOLTAGE SELECT***

P3 is a 3-pin .1" single row header. It is used to select between 6V or 12V (in series mode) tube heaters.

### ***8.5 RP1 AND RP3 TRIMPOTS***

RP1 and RP3 are the bias adjustment potentiometers for the Left and Right Channels respectively.

### ***8.6 RP5 –VOLUME POT WITH ON/OFF SWITCH***

RP5 is an Alps RK09 Low Noise, Conductive Plastic Volume Control with built-in On/Off Switch.

### ***8.7 SW1 – ATTENUATION SWITCH***

SW1 – a Single Pole, Double Throw (SPDT) toggle switch that controls the attenuation relay.

### ***8.8 SW2 – OUTPUT RESISTANCE SLIDE SWITCH***

SW2 is a Double Pole, Three Position (DP3T) Slide Switch. It adds 0, 47 and 100 ohm headphone output resistance when in the Left, Middle and Right positions respectively.



## **9 DOCUMENT REVISIONS**

Date	Revision	Change
10/6/2016	P5	Preliminary Release

**Table 4 – Document Revisions**

# **IO ERRATA**

## ***10.1 OVERVIEW***

There are currently no known errata for the 503HTA Rev. P1.